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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/606,159

06/29/2000

Takaaki Nagai

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1550

22428

7590

10/29/2003

FOLEY AND LARDNER

SUITE 500

3000 K STREET NW

WASHINGTON, DC 20007

EXAMINER

BROCK II, PAUL E

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/606,159

Applicant(s)

NAGAI ET AL.

Examiner

Paul E Brock II

Art Unit

2815

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-24 and 26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 24 and 26 is/are allowed.
- 6) ☒ Claim(s) 21-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 June 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/124,851.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 21 – 24 and 26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. With regard to claims 21 and 24, it is not clear in the 5th line of the claim to what “a plurality of memory cell transistors and a plurality of memory transistors” corresponds. Are there both memory cell transistors and memory transistors? How are these two types of transistors related? For purposes of this office action “a plurality of memory cell transistors and a plurality of memory transistors” will be considered --a plurality of memory cell transistors--.

4. Claim 23 recites the limitation "said first and second metal wiring layers" in the first and second line of the claim. There is insufficient antecedent basis for this limitation in the claim. For purposes of this office action "said first and second metal wiring layers" will be considered --said first metal wiring layer--.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 21 is rejected under 35 U.S.C. 102(b) as being anticipated by the applicant's admitted prior art (AAPA).

The AAPA discloses in figures 1 – 2 and 5 – 8d a method of fabricating an EEPROM semiconductor device having a plurality of memory cell transistors in figures 1 – 7. The AAPA discloses in figure 2 forming a plurality of field insulating films (3) in parallel with one another in a first direction on a semiconductor substrate, each of the plurality of field insulating films provided for a plurality of memory cell transistors formed between two associated adjacent field insulating films. The AAPA discloses in figure 8a forming a first gate insulating film (4) in each of active regions. The AAPA discloses in figures 2 and 8a forming a plurality of first polysilicon film. The AAPA discloses in figure 2, figure 8a and page 2, lines 5 – 13 patterning the first polysilicon film to form first polysilicon strips (5a) in parallel with one another, the first polysilicon strips formed in the first direction. The AAPA discloses in figure 8a forming a second gate insulating film (6) on the first polysilicon strips. The AAPA discloses in figure 8a forming a second polysilicon layer (7a) on the second gate insulating film. The AAPA discloses in figure 8b and page 5, lines 16 – 21 patterning the second polysilicon layer, the second gate insulating film, the first polysilicon strips and the first gate insulating film to form a plurality of

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control gates (7), a plurality of second gate insulators (6), a plurality of floating gates (5), and a plurality of first gate insulators (4), respectively. The AAPA discloses in figure 8b and page 5, lines 16 – 21 forming drain (8a) and source (8b) regions. The AAPA discloses in figure 8c and page 5, lines 23 – 26 forming a first interlayer insulating layer (10) on an entire surface of the semiconductor substrate. The AAPA discloses in figure 8c and page 5, lines 26 – 28 forming contact-holes (C1 and C2) through the first interlayer insulating layer in alignment with the drain and source regions. The AAPA discloses in figure 8d and page 5, line 29 – page 3, line 9 forming a first metal wiring layer (17a and 17b) on the first interlayer insulating layer and filling the contact-holes therewith to couple the first wiring layer to a corresponding one of the drain and source regions in a memory area and a wiring layer of a logic area.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA as applied to claim 21 above, and further in view of Kamiya et al. (USPAT 5838615, Kamiya).

With regard to claim 22, the AAPA discloses in figure 8a a second gate insulating film. The AAPA does not teach a material for the second insulating film. Kamiya discloses in column 4, lines 46 – 51 that a second gate insulating film has a three-layer structure of

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oxide/nitride/oxide films. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the second gate insulating film of Kamiya in the method of the AAPA in order to use a material that is well known in the art to use as a second dielectric layer.

5. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over the AAPA as applied to claim 21 above, and further in view of Yonemoto (USPAT 5506434).

The AAPA discloses on page 6, lines 6 – 9 that the first metal wiring layers are composed of a refractory metal. The AAPA does not teach that the first metal wiring layer is composed of aluminum. Yonemoto teaches forming a first wiring layer composed of aluminum in column 5, lines 8 – 11. It would have been obvious to use the aluminum wiring of Yonemoto in the process of the AAPA in order to form signal lines to connect to the source region as stated by Yonemoto in column 5, lines 8 – 11. These signal lines of aluminum will have higher conductivity than signal lines formed of a refractory metal.

Allowable Subject Matter

6. Claims 24 and 26 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record does not disclose or suggest at least the limitation of “forming aluminum

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backing wiring layers connecting to said plurality of control gates, simultaneously with forming said common source line.”

Response to Arguments

8. Applicant's arguments with respect to claims 21 – 23 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703) 308-6236. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
October 21, 2003

A handwritten signature in black ink, appearing to read "Paul E Brock II", with a stylized flourish at the end.